2664 /m

Docket No.: 50100-786

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

John CHIANG, et al. :

Serial No.: 09/304,964 : Group Art Unit: 2664

Filed: May 05, 1999 : Examiner: K. Yao

For: DYNAMIC TIME SLOT ALLOCATION IN INTERNAL RULES CHECKER SCHEDULER

REQUEST FOR RECONSIDERATION

Commissioner for Patents
Washington, DC 20231

Sir:

This Request is submitted in response to the Office Action mailed November 2, 2001.

Claims 1-18 have been rejected under doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. patent issued on the U.S. application No. 09/304,959.

First, it is noted that this rejection is improper because U.S. patent No. 6,335,938 was issued on application No. 09/304,959 after the mailing date of the Office Action. Accordingly, the Examiner had to apply a provisional rejection.

Second, it is well settled that any analysis employed in an obviousness-type double patenting rejection parallels the guidelines for analysis of a 35 U.S.C. 103 obviousness determination. ***In re Braat,*** 937 F.2d 589, 19 USPQ2d 1289 (Fed. Cir. 1991).

As stated in ***Graham v. John Deere Co.*** 383 U.S. 1, 13, 148 U.S.P.Q. 459, 465 (1966), obviousness under 35 U.S.C. §103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art. The Examiner should recognize that the fact that the prior art *could* be modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. ***In re Deminski***, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). In the absence of such a prior art suggestion for modification of the references, the basis of the rejection is no more than inappropriate hindsight reconstruction using applicants' claims as a guide. ***In re Warner***, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

Applicants respectfully submit that the Examiner has improperly applied hindsight as a basis for a holding of obviousness.

In particular, independent claims 1 and 11 of U.S. patent No. 6,335,938 recite dynamically distributing the expansion port and high-speed port time slots between the expansion port and the high-speed port in accordance with relative data traffic at the expansion port and the high-speed port.

Hence, time slots for expansion port and high-speed port are distributed between respective ports.

By contrast, claims 1 and 12 of the present application recite dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports.

It is respectfully submitted that one skilled in the art would have no reason to arrive at the invention claimed in the present application based on the distribution of slots between expansion port and high-speed port.

Accordingly, the Examiner's conclusion of obviousness is not warranted.

Further, claims 1-18 have been rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. This rejection is respectfully traversed for the following reasons.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The initial burden of establishing a basis for denying patentability to a claimed invention rests upon the Examiner. ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***In re Thorpe***, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985); ***In re Piasecki***, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). To satisfy this burden, therefore, each and every element of the claimed invention must be shown by the Examiner to be disclosed in Wu et al.

Applicant respectfully asserts that the record fails to meet this requirement.

In particular, independent claim 1 recites a multiport data communication system for switching data packets between ports. The data communication system comprises a plurality of receive ports for receiving data packets, and a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port.

The decision making engine includes:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports.

It is respectfully submitted that the Examiner did not point out wherein the reference discloses the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports.

Considering the rejection, it appears that the Examiner considers the processor for receiving data cells from the FIFO to correspond to the claimed decision making engine.

However, the reference does not disclose that this processor comprise a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports, logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports.

Instead, Wu et al. discloses scheduling cells of multiple communications for transmission in an ATM communications system. The cells are assigned time slots based on the priority of the cells.

Further, independent claim 12 recites a method of data processing comprising the steps of:

placing data blocks representing received data packets in a plurality of data queues corresponding to the plurality of the receive ports,

transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports.

The Examiner did not address these steps. However, it is submitted that the reference does not describe the steps recited in claim 12.

Moreover, the Examiner failed to address limitations of dependent claims 2-11, and 13-18. It is respectfully submitted that Wu et al. does not disclose the subject matter of these claims.

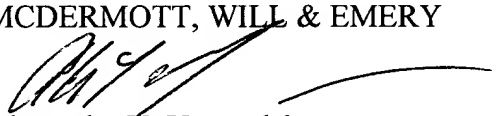
Hence, the Examiner's rejection of claims 1-18 under 35 U.S.C. 102 is improper and should be withdrawn.

In view of the foregoing, and in summary, claims 1-18 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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